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Remarks

Reconsideration of this Application is respectfully requested. Based on the remarks set forth below, it is respectfully requested that the Examiner reconsider and withdraw all outstanding rejections.

Rejection under 35 U.S.C. § 102

The Examiner, on page 2 of the Final Office Action, states that claims 1, 4, 6-7, 9-13, 15, 17-20, 22-24, 26, and 27 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,757,811 to Mukherjee. Applicants respectfully traverse this rejection. Based on the remarks set forth below, Applicants respectfully request that this rejection be reconsidered and withdrawn.

To anticipate a claim of a pending application, a single reference must disclose each and every element of the claimed invention. *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1397 (Fed. Cir. 1986). The exclusion of a claimed element from the single source is enough to negate anticipation by that reference. *Atlas Powder Co. v. E.I. du Pont de Nemours & Co.*, 750 F.2d 1569, 1574 (Fed. Cir. 1984).

With respect to independent claim 1, the Examiner states that Mukherjee teaches every element of Applicants' claimed invention. Applicants respectfully disagree.

Contrary to the present invention, Mukherjee does not teach or suggest every element of Applicants' invention. For example, referring to independent claim 1, Mukherjee does not teach or suggest at least the following claimed element of "a data value prediction module coupled to the second pipeline."

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The present invention teaches a run-ahead pipeline that functions by issuing load operations to the data cache. If there is a cache miss, such that the data to be obtained has not already been loaded from the main memory into the data cache, the missing value will be predicted using a value prediction module. Thus, instead of waiting for the data cache to load a value from main memory when a data cache miss occurs, the run-ahead pipeline continues execution of the run-ahead thread using the predicted value. The predicted values are never stored to memory or the data cache. See Specification, page 4, lines 17-21; page 4, line 31 – page 5, line 4; page 6, lines 20-30.

Unlike the present invention, Mukherjee does not teach a value prediction module, and is silent on predicting the missing value. To the contrary, Mukherjee appears to teach that a value from main memory is loaded into the data cache when a data cache miss occurs. See Murkherjee, col. 7, lines 53-55, stating that "[s]ome or all cache misses in the leading thread will result in the requested data being written to the processor's data cache." Thus, with Mukherjee, a cache miss processed in the leading thread eliminates a corresponding cache miss in the trailing thread by storing the requested data in the cache during processing of the leading thread. Id. In fact, Mukherjee teaches away from Applicants' element of "a data value prediction module coupled to the second pipeline" because Mukherjee allows the leading thread to resolve the cache miss by storing the requested data in the data cache so that the corresponding instructions in the trailing thread will not experience the cache miss. Thus, with Mukherjee there is no need to have a data value prediction module because the missing cache value is retrieved from main memory and stored in the data cache.

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For at least these reasons, Applicants respectfully submit that Mukherjee does not include each and every element of Applicants' claimed invention as recited in independent claim 1. Independent claim 13 recites similar elements to claim 1. Therefore, independent claims 1 and 13, and the claims that depend therefrom (claims 2-12 and 14-19, respectively), are patentable over Mukherjee.

With regards to claim 20, Mukherjee does not teach or suggest at least the following element of "calculating a predicted load value for execution of the LOAD instruction if a cache miss in the data cache results when the second pipeline executes the LOAD instruction before the first pipeline." Unlike the present invention, which supplies a predicted value for the load value instead of an actual value retrieved from memory, Mukherjee does not need to predict a load value because Mukherjee actually resolves the cache miss with the leading thread by retrieving the actual value from memory and storing it in the cache so that the corresponding instructions in the trailing thread will not experience the cache miss.

Thus, for at least these reasons, Applicants respectfully submit that Mukherjee does not include each and every element of Applicants' claimed invention as recited in independent claim 20. Independent claim 24 includes similar elements to claim 20. Therefore, independent claims 20 and 24, and the claims that depend therefrom (claims 21-23 and 25-27, respectively), are patentable over Mukherjee.

Applicants respectfully request that the Examiner reconsider claims 1, 13, 20, and 24, and the claims that depend therefrom, and withdraw this rejection.

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Rejection under 35 U.S.C. § 103

The Examiner, on page 10 of the Office Action, states that claims 2-3, 5, and 14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,757,811 to Mukherjee. Applicants respectfully traverse this rejection. Based on the remarks set forth below, Applicants respectfully request that this rejection be reconsidered and withdrawn.

Claims 2-3 and 5 depend from independent claim 1, which is patentable over Mukherjee for at least the reasons stated above. Applicants therefore respectfully request that the Examiner reconsider and withdraw the rejection of dependent claims 2-3 and 5.

Claim 14 depends from independent claim 13, which is patentable over Mukherjee for at least the reasons stated above. Applicants therefore respectfully request that the Examiner reconsider and withdraw the rejection of dependent claim 14.

The Examiner, on page 12 of the Office Action, states that claims 8, 16, 21, and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,757,811 to Mukherjhee in view of "Improving CC-NUMA Performance using Instruction-based Prediction," by Kaxiras *et al.* (hereinafter referred to as "Kaxiras"). Applicants respectfully traverse this rejection. Based on the remarks set forth below, Applicants respectfully request that this rejection be reconsidered and withdrawn.

Claim 8 depends from independent claim 1, which is patentable over Mukherjee for at least the reasons stated above. Applicants therefore respectfully request that the Examiner reconsider and withdraw the rejection of dependent claim 8.

Claim 16 depends from independent claim 13, which is patentable over Mukherjee for at least the reasons stated above. Applicants therefore respectfully request that the Examiner reconsider and withdraw the rejection of dependent claim 16.

Claim 21 depends from independent claim 20, which is patentable over Mukherjee for at least the reasons stated above. Applicants therefore respectfully request that the Examiner reconsider and withdraw the rejection of dependent claim 21.

Claim 25 depends from independent claim 24, which is patentable over Mukherjee for at least the reasons stated above. Applicants therefore respectfully request that the Examiner reconsider and withdraw the rejection of dependent claim 25.

Further, the M.P.E.P. states that "[t]he Examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the Examiner does not produce a *prima facie* case, the Applicant is under no obligation to submit evidence of nonobviousness." M.P.E.P. § 2142, page 2100-123.

Applicants respectfully assert that the obviousness rejection is improper because the Examiner has not established a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves, or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." M.P.E.P. § 2141, page 124. Applicant asserts that there is no suggestion or motivation in the references themselves or in the knowledge of one skilled in the art, to modify the reference or to combine reference teachings. As indicated above, Mukherjee does not need to predict a load value because Mukherjee actually resolves the cache miss with the leading thread by retrieving the actual value from memory and storing it in the cache so that the

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corresponding instructions in the trailing thread will not experience the cache miss.

Thus, for at least these reasons, Applicants assert that Mukherjee does not suggest being combined with Kaxiras. Therefore, this obviousness rejection is improper.

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Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all currently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Response is respectfully requested.

Respectfully submitted,

Intel Corporation

Dated: April 13, 2005

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